REMARKS

Claims 1-11 and 13-16 are pending in the application.

Claim 8 is allowed.

Claims 1-7, 9-11 and 13-16 are rejected.

Claims 1-4 are rejected under 35 U.S.C. 102(b).

Claims 1-4 and 10-16 are rejected under 35 U.S.C. 102(b).

Claims 5-7 and 9 are rejected under 35 U.S.C. 103(a).

Claims 1, 5 and 10 are currently amended with no new matter added.

Claim Rejections – 35 U.S.C. § 102

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano Atsushi (JP 6-140355), hereinafter called "Atsushi."

Applicants respectfully traverse the rejections.

Claim 1 has been amended to recite additional limitations to overcome Atsushi. Claim 1 now includes forming a gate insulation layer formed on a semiconductor substrate; forming a floating gate electrode formed on the gate insulation layer; and forming an intergate dielectric layer formed on the floating gate electrode. Support for this amendment can be found, among other locations, on page 7, lines 16-17 of the Specification, and FIG. 4.

Atsushi does not include the added limitations of claim 1. In Atsushi's constitution and the accompanying figure, he fails to show a gate insulation layer, a floating gate electrode, and an intergate dielectric layer.

Atsushi, failing to show or teach all of its elements, fails to anticipate claim 1. Therefore, applicants request reconsideration and allowance of claim 1.

Also, claims 2-4, depending from claim 1, each recite additional limitations, and are therefore also in condition for allowance.

Claims 1-4 and 10-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang, et al. (U.S. Pat. 6,180,454), hereinafter called "Chang."

Applicants respectfully traverse the rejections.

Claim 1 has been amended to recite (among other things) an amorphous silicon capping layer being formed *directly* on a polysilicon layer after forming the polysilicon layer. FIG. 4 in the Specification, for example, shows an amorphous silicon capping layer 38b directly on a polysilicon layer 38a (see also page 7, lines 19-20).

Chang does not teach or show an amorphous silicon capping layer *directly* on a polysilicon layer. Chang, in FIG. 3D, for instance, shows a poly 1 layer 44 and a poly 2 layer 48. The poly 1 or poly 2 layers can be either amorphous silicon or polysilicon, but not both. Chang makes this point clear in col. 5, lines 33-35, when he states that polysilicon is used *instead* of amorphous silicon in another embodiment. Here, Chang also explains "the *term* poly 1 (or poly 2) includes both amorphous silicon layers and polysilicon layers" (emphasis added). In other words, poly 1 or poly 2 may be formed of *either* amorphous silicon or polysilicon, but not both. Please note the use of the word "term." The above description of Chang does not state that poly 1 (or poly 2) *itself* includes both amorphous silicon layers and polysilicon layers. Chang is only defining the meaning of the term poly 1 (and poly 2).

In other words, Chang does not teach an amorphous silicon capping layer directly on a polysilicon layer because the poly 2 layer 48 (or the poly 1 layer 44) only consists of amorphous silicon or polysilicon, but not both. The recitation of claim 1 requires that *both* amorphous silicon *and* polysilicon be present.

Chang does include the possibility that the poly 1 layer 44 is a polysilicon layer while the poly 2 layer 48 is an amorphous silicon layer. Even in this case, however, Chang is not teaching an amorphous silicon layer *directly* on a polysilicon layer, because of the intervening dielectric layer 46.

To further the point that the poly 1 or poly 2 layers are either amorphous silicon or polysilicon, but not both, Chang, in col. 9, line 66 to col. 10, line 8 states that "a phosphorus in situ doped amorphous silicon layer is deposited via LPCVD ..... *Alternatively*, a doped polysilicon layer may be formed as the poly 1 layer." Emphasis has been added to point out the word "Alternatively."

Claim 10 also has been amended to recite an amorphous silicon capping layer *directly* on a polysilicon layer. As explained above regarding claim 1, Chang does not teach or show this limitation.

For at least the reasons explained above, Chang does not teach the structural relationships or limitations of claims 1 and 10. Therefore, applicants request reconsideration and allowance of these claims.

Claims 2-4 depend from claim 1 and inherently include all of the limitations of this base claim. Claims 11 and 13-16 depend from claim 10 and inherently include all of the limitations of this base claim. As discussed above, the prior art does not teach the limitations of these base claims much less the further embodiments of their respective dependent claims.

Therefore, claims 2-4, 11, and 13-16 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Claim Rejections – 35 U.S.C. § 103

Claims 5-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Pat. 6,180,454) in view of Oka, et al. (U.S. Pat. 6,235,563), hereinafter called "Oka."

Applicants respectfully traverse the rejections.

Claim 5 also has been amended to recite an amorphous silicon capping layer *directly* on a polysilicon layer. As explained above regarding claim 1, Chang does not teach or show this limitation.

Also, Oka fails to make up for Chang's deficiencies, and their combination does not anticipate or render obvious all of the limitations and elements of claim 5. Therefore, applicants request reconsideration and allowance of claim 5.

Claims 6-7 and 9 depend from claim 5 and inherently include all of the limitations of this base claim. As discussed above, the prior art does not teach the limitations of this base claim much less the further embodiments of the dependent claims. Therefore, claims 6-7 and 9 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Allowable Subject Matter

Applicants thank the Examiner for recognizing that claim 8 is allowable.

For the foregoing reasons, reconsideration and allowance of claims 1-7, 9-11 and 13-16 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on October 26, 2005.

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